REMARKS

Claims 1-40 are pending in the present application. Claim 10 has been cancelled. Claims 1, 8, 16, and 27 have been amended. Applicant respectfully requests entry of the foregoing amendments to Claims 1, 8, 16, and 27 prior to further examination. No new matter has been introduced.

Allowable Subject Matter

The Applicant thanks the Examiner for the indication of allowable subject matter in other claims.

The Examiner stated that Claims 36-38 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. Applicant has not amended claims 36-38 because Applicant believes, for the reasons set forth blow, that amended base Claim 27 is allowable.

Claim Amendments

Applicant has amended Claims 1, 8, 16, and 27 to include features related to the second data interface unit/access path having priority over the first data interface unit/access path. Support for these claim amendments can be found at least in the Specification on page 23, line 12 through page 26, line 20; FIGS. 10 and 11; and originally filed Claim 10.

Present Invention

By way of example with reference to Figs. 10 and 11, the presently claimed invention teaches a memory subsystem equipped with a first data transfer interface 1106a coupled to an array of memory cells 1102 to provide a first access path for a processor and a subsystem, a second data transfer interface coupled to the array of memory cells to provide a second access path 112 for the processor to access the array of memory cells, and a controller coupled to the array of memory cells and the first and second data transfer interfaces to control access to the array of memory cells. That is, access is granted to the second data transfer interface prior to granting access to the first data transfer interface.

Regarding Section 102 Rejections

Claims 1-4, 6-9, 11-20, 22-26, and 39 have been rejected under 35 U.S.C. § 102(e) as being anticipated by Chen (U.S. Patent No. 5,197,130). The rejection is respectfully traversed.

Chen describes a cluster architecture for a highly parallel multiprocessor computer processing system. The system includes one or more clusters of tightly-coupled, high-speed processors capable of both vector and scalar parallel processing that can symmetrically access shared resources associated with the cluster, as well as the shared resources associated with other clusters. Chen does not teach a second data interface having priority over the first data transfer interface. In contrast, Chen describes a "first-come-first-served" priority scheme and although this scheme includes priority data, it in no way suggests priority is given to the second data interface over the first data interface. Rather, Chen would use the highest priority request no matter where the request came from.

Chen does not teach, suggest, or otherwise make obvious "a second data transfer interface coupled to the array of memory cells to provide a second access path for said processor to access said array of memory cells, the second data transfer interface having priority over the first data transfer interface" as now claimed in amended Claim 1. Applicant respectfully requests the withdrawal of the rejection of amended Claim 1 under section 102.

Dependent claims 2-4, 6, 7, and 39 depend from allowable base Claim 1 and are allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of dependent Claims 2-4, 6, 7, and 39 under section 102.

Independent Claims 8, 16, and 27 have been amended to include similar limitations as now claimed in amended Claim 1 and are allowable for the same reasons. Claims 9, 11-15 depend from amended Claim 8 and Claims 17-20 and 22-26 depend from amended Claim 16 and are allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of amended Claims 8-9, 11-20, and 22-27 under section 102.

Regarding Section 103 Rejections

Claims 27-29 and 31-35 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen.

As stated above, Claim 27 has been amended to include similar limitations as claimed in amended Claim 1, namely "the memory unit servicing said second memory accesses made through said second access path prior to servicing said first memory accesses made through said first access path." Chen does not teach, suggest, or otherwise, alone or in combination, this claim limitation. Claims 28, 29, and 31-35 are dependent from amended Claim 27 and are allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of amended Claim 27 and dependent Claims 28, 29, and 31-35 under section 103.

Claim 40 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Mulla (U.S. Patent No. 6,557,078).

Mulla describes a cache using a queuing structure that provides out-of-order cache memory access support for multiple accesses, as well as support for managing bank conflicts and address conflicts. Mulla does not teach a second data interface having priority over the first data transfer interface.

As stated above, Claim 1 has been amended to include "a second data transfer interface coupled to the array of memory cells to provide a second access path for said processor to access said array of memory cells, the second data transfer interface having priority over the first data transfer interface". Chen and Mulla, alone or in combination, does not teach, suggest, or otherwise make obvious this limitation. Claim 40 depends from amended Claim 1 and is allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of Claim 40 under section 103.

Claims 5, 10, 21, and 30 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Agarwala (U.S. Patent No. 6,681,270). Claim 10 is herein cancelled.

Agarwala describes a data transfer controller that uses an effective channel priority processing technique and algorithm. Data transfer requests are queued in a first-in-first-out

fashion at the data source ports. This technique prevents a low priority data transfer request at the output of a source port queue from blocking a higher priority data transfer request further back in the same port. Agarwala does not teach a second data interface having priority over the first data transfer interface. In contrast, like Chen, Agarwala utilizes a "first-in-first-out" priority scheme and although this scheme includes priority data, it in no way suggests priority is given to the second data interface over the first data interface. Rather, Agarwala would use the highest priority request no matter where the request came from.

Neither Chen or Agarwala, alone or in combination, teaches, suggests, or otherwise makes obvious the limitations as now claimed in amended Claim 1. Claim 5 depends from amended Claim 1 and is allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of Claim 5 under section 103.

Independent Claims 16 and 27 have been amended to include similar limitations as now claimed in amended Claim 1 and are allowable for the same reasons. Claims 21 and 30 depend from amended Claims 16 and 27, respectively and are allowable for the same reasons. Applicant respectfully requests the withdrawal of the rejection of amended Claims 16 and 27 under section 103.

Information Disclosure Statement

A Supplemental Information Disclosure Statement (SIDS) is being filed concurrently herewith. Entry of the IDS is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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